

MATTEL ELECTRONICS

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Intellivision Keyboard Quality

o Total in market		498 units
o Units sold Seattle market		45 units
o Total sold New Orleans		<u>75 units</u>
o Total sold to date		120 units
o Gross return rate	10.0%	(12 units)
o Accessories return rate	5.00%	(6 units)
o Software return rate	.83%	(1 units)
o Non-Defectives	0%	(0 units)
o Keyboard return rate	4.16%	(5 units)



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Intellivision Keyboard Quality

Market Research Distribution

July 15, 1981

o 1'st distribution		68 units
o Gross return rate	32.35%	(22 units)
o Accessories return rate	10.29%	(7 units)
o Defective software	1.47%	(1 units)
o Non-Defective	1.47%	(1 units)
o Keyboard return rate	19.1%	(13 units)



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Intellivision Keyboard Quality

Market Research Distribution

August 26, 1981

o 2'nd distribution		66 units
o Gross returns rate	21.21%	(14 units)
o Accessories return rate	4.54%	(3 units)
o Defective software	4.54%	(3 units)
o Non-Defective	1.52%	(1 units)
o Keyboard return rate	10.00%	(7 units)



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INTELLIVISION KEYBOARD QUALITY

LIFE TEST RESULTS TO DATE	
O 100HRS. GROSS FAILURES	31.25%
O TAPE STALLS AND TORQUE ADJ.	25.00%
O TORQUE ADJUSTMENT	6.25%
O 200 HRS GROSS FAILURES	37.50%
O REPEATED FAILURES	31.25%
O TAPE STALLS	25.00%
OWILL NOT LOAD "M" TAPE	6.25%
O NEW FAILURE CPU -2	6.25%
O 300 HRS GROSS FAILURES	6.25%
O TAPE STALLS	6.25%
O 500 HRS GROSS FAILURES	31.25%
O TAPE STALLS	31.25%

THE 100HOUR FAILURES WERE REPAIRED AND REPLACED BACK INTO LIFE TEST AFTER EACH FAILURE.

THESE UNITS ALSO FAILED AT $300\frac{1}{2}$ HOURS AND AT THE 500HOUR POINTS

D.BOWEN 11-23-81



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KEYBOARD OVERVIEW FEBRUARY 8, 1982

1. Present Status
2. Cost Reduction Plan
3. Manufacturing Proposal



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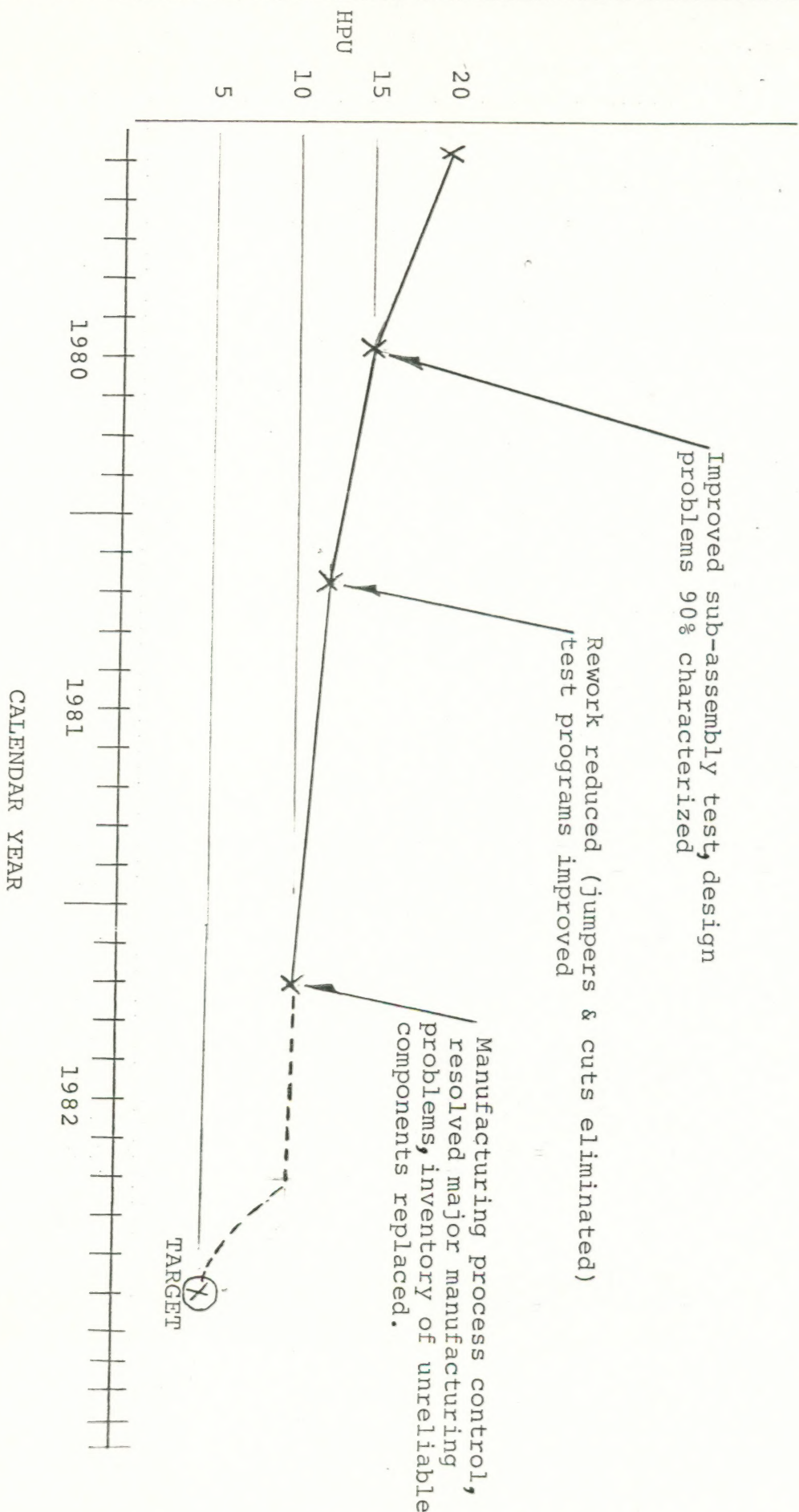
P R E S E N T K E Y B O A R D S T A T U S

- Manufacturing Costs \$506 to \$530 per unit
- Highly Labor Intensive (10 Hours Per Unit)
- Difficult Manufacturing Process
- Incomplete and Inadequate Test Programs
- Poor Quality of Finished Product (30% return test toy)
- Complexity is approximately 10 times greater than Master Component



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LABOR HOURS PER UNIT (HPU) VS TIME



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Poor Quality And Higher Cost Are Related

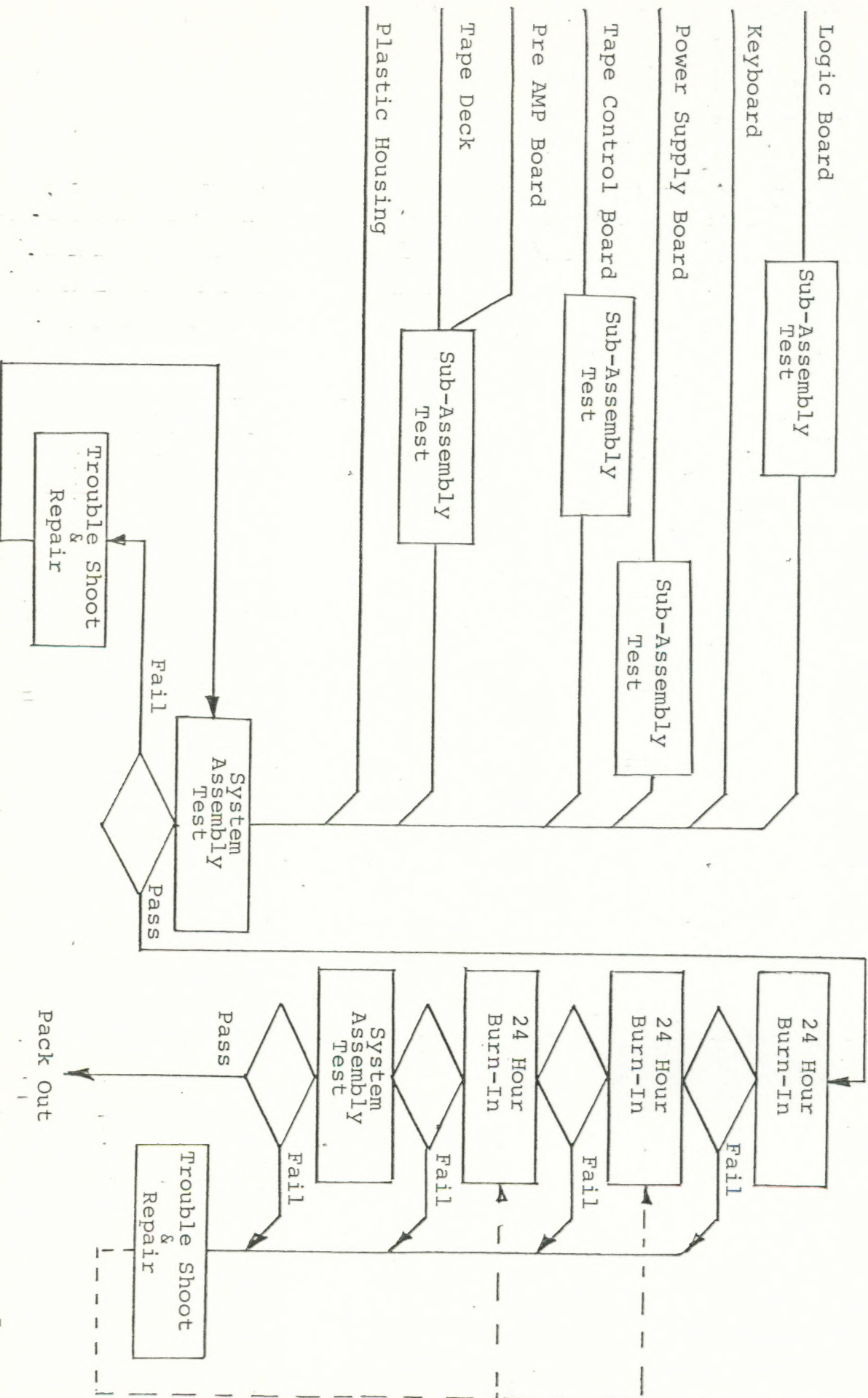
Improving The Quality Will Also Reduce Cost

Method of Improvement

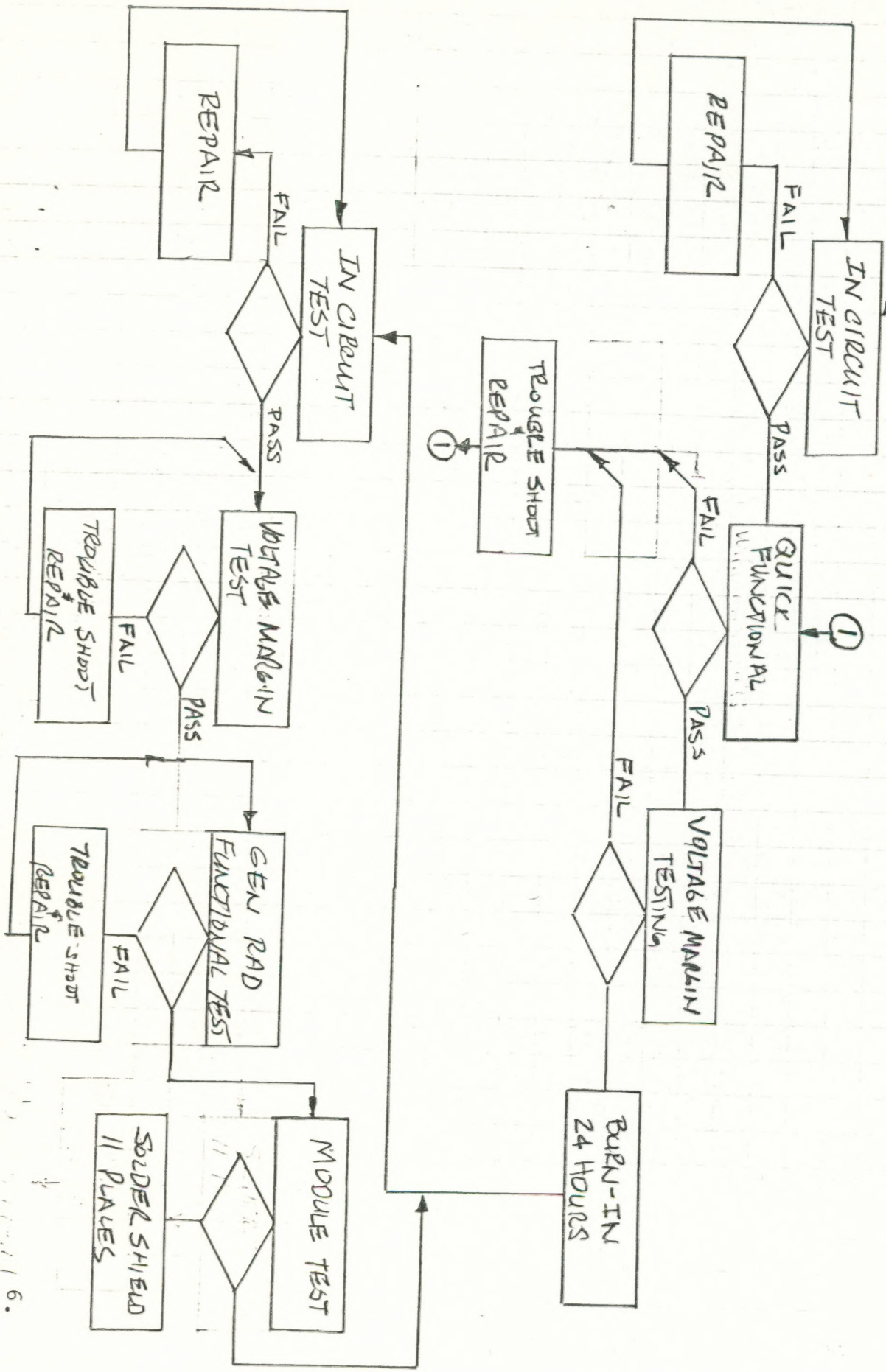
1. Control the quality of material
2. Motivate control of the assembly process
 - Instill a quality attitude
 - Provide assembly feedback on a timely basis
3. Improve the test function
 - Reduce the number of test escapes
 - Improve interchangeability by adding margin testing
 - Eliminate inconclusive test results
 - Install a "TEST DISCIPLINE"



KEYBOARD COMPONENT ASSEMBLY & BURN-IN



ASSY & INSPECTION LOGIC BOARD SUB ASSEMBLY TEST



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4 0 0 0 U N I T B U I L D S T R A T E G Y

Design Changes - Minimized: correct only functional essentials

Procurement - No deviations from approved vendor list

All components requiring burn-in to be burned-in
Printed circuit vendors approved - proven performance

Process - Remove Master Component from high temp burn-in

Burn-in logic board prior to system burn-in
Require all subassemblies to be in-circuit-tested

Test - Improve in-circuit-test (correct known deficiencies)

Add a logic board functional test after in-circuit-test
Add voltage-margin testing of logic board



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4000 UNIT BUILD SCHEDULE

Week Beginning	<u>APRIL</u>					<u>MAY</u>				<u>JUNE</u>	
	29	5	12	19	26	3	10	17	24	31	7 14
Quantity Per Week	500	500	500	500	500	500	500	500	500		
Cum Quantity	500	1000	1500	2000	2500	3000	3500	4000	4500		

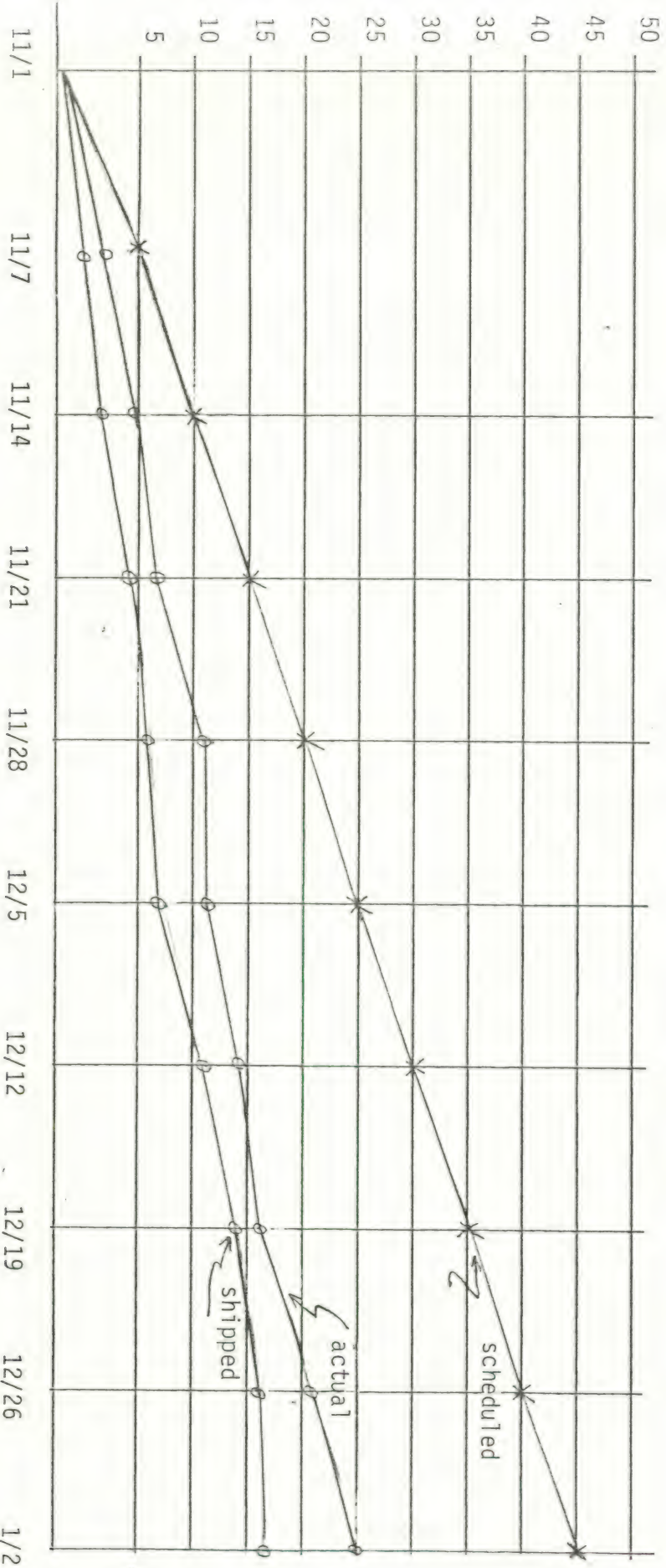
Key Requirements to Accomplish Schedule (4000 by 6-1-82)

1. In-circuit tester on site
2. Two (2) Gen Rad functional testers on site
3. ALL materials at site by March 15, 1982
4. Run rate of 100 per day achieved by April 1, 1982
5. Burn-in racks must be capable of 135/day capacity
6. Manufacturing personnel ramp up accomplished to support the schedule.
7. Mattel Engineering support readily available (≤ 1 hr travel time)



GRAND X START-UP 1981

- 2 GTE technicians on board in August
- Entire facility equipped & Fairchild tester installed in August
- Sample quantities of PCB & other assemblies manufactured in September
- Material available for production start November



June 2, 1982

DAVE
CHANDLER
FYI tax hugh 6/3

TO: Distribtuion
FORM: John H. Lishman JHL
SUBJECT: KEYBOARD COMPONENT DRAWING LIST,
1149-5892, Rev. "A", dated 6/01/82
Reference: 078/JHL/82

Attached is a copy of the Keyboard Component drawing list, updated as of 6/01/82.

JHL/jk

Distribution - w/attachment

Ricardo Bailey
Bob Baird
Hugh Barnes
B. Bornina
Dave Danner

John Fairbanks
Anita Hollensed
Frank Levine
Wilson Quan
Mac McAlister

Diana Reichman
Dick Shaffer
Ward Spaniol
Floyd Teter
Ed Yee

RECEIVED
JUN -4 1982
D. CHANDLER

<u>DRAWING NUMBER</u>	<u>REV</u>	<u>SHEETS</u>	<u>DWG SIZE</u>	<u>NOMENCLATURE</u>
1149-9991	PR	3	D	KEYBOARD COMPONENT TOP ASSEMBLY
1149-5999	B	39	A	PRODUCT SPECIFICATION, KEYBOARD COMP
PL 1149-9991	X	7	A	PARTS LIST, KEYBOARD COMPONENT SYSTEMS LEVEL
1149-5829	A	3	A	KEYBOARD COMPONENT DOCUMENT CONTROL LIST
TS 1149-5649	C	31	A	SYSTEM LEVEL TEST PROCEDURE
TS 1149-5879	B	18	A	KEYBOARD COMPONENT BURN IN PROCEDURE
TS 1149-5789	PR	3	A	KEYBOARD COMPONENT HIGH POT TEST
1149-2119	P	2	E	UPPER HOUSING
1149-4399	PR	1	B	INLAY
1149-0880	A	1	B	CAUTION LABEL
1149-9129	F	1	F	TAPE DECK ASSEMBLY
PS 1149-4129	PR	32	A	PROCUREMENT SPEC, CASSETTE DRIVE
TS 1149-5659	D	15	A	TAPE DECK ASSEMBLY MODULE TEST
TS 1149-5709	D	8	A	CASSETTE DRIVE SUBASSEMBLY ACCEPTANCE TEST
TS 1149-5719	C	5	A	EOT TEST PROCEDURE
1149-2129	F	1	D	TAPE COVER
1149-9169	C	1	C	EOT SENSOR ASSEMBLY
1149-4279 *	PR	1		ALIGNMENT POST
1149-9649 *	PR	1		FOIL, ALIGNMENT POST
1149-4079 *	PR	1	B	CLUTCH BELT
1149-4089 *	PR	1	A	FLYWHEEL BELT
1149-4029	PR	1	C	PROTECTIVE PLATE
1149-4209	B	1	C	CASSETTE SPRING
1149-4339	A	1	C	PREAMP RF SHIELD
1149-4479	D	1	B	RH BRACKET
1149-4469	C	1	B	LH BRACKET
1149-9199	E	1	D	PREAMP ASSEMBLY
PL 1149-9199	B	3	A	PARTS LIST, PREAMP ASSEMBLY
1149-6199	A	4	C	PCB FAB DETAIL, PREAMP ASSEMBLY
1149-3199	C	1	D	SCHEMATIC, PREAMP ASSEMBLY
1149-7659	PR	1	B	RIBBON CABLE ASSEMBLY, LOGIC NINE CONDUCTOR
1149-2159	PR	1	D	STRAIN RELIEF BAR
0405-0536	PR	1	A	SCREW, 5-40 X 1/4
0405-0625	A	1	A	SCREW, 2.6mm X 3.0 mm.
0405-0526	PR	1	A	SCREW, 5-40 X 5/8
0405-0974	PR	1		SPACER, NYLON, 1/4 THICK
0089-0029	PR	1	B	TAB, MALE, 0.25in., ANTI ROTATIONAL
0405-0784	PR	1		CABLE TIE, 3 INCHES.
0089-0817	PR	2	A	SHRINK TUBING
0405-0304	PR	1		SCREW, 10-16 X 1/2
0089-0451	A	1	A	WIRE, TWISTED PAIR, BLACK/YELLOW
0089-0453	A	1	A	WIRE, TWISTED PAIR, YELLOW/RED
0089-0454	A	1	A	WIRE, TWISTED PAIR, RED/BLUE
0089-0455	PR	1	A	WIRE, PREPARED, RED
0089-0456	PR	1	A	WIRE, PREPARED, BLACK
0089-0457	A	1	A	WIRE, TWISTED PAIR, BLUE/YELLOW
0089-0458	A	1	A	WIRE, TWISTED PAIR, BLACK/RED

*NORMALLY SUPPLIED AS PART OF NEXT HIGHER ASSEMBLY

<u>DRAWING NUMBER</u>	<u>REV</u>	<u>SHEETS</u>	<u>DWG.SIZE</u>	<u>NOMENCLATURE</u>
1149-9349	PR	1	D	KEYBOARD ASSY 60 STATION
PS 1149-9349	PR	9	A	PROCUREMENT SPEC,KYBD ASSY
TS 1149-5749	PR	2	A	KEYBOARD ASSY MINI TEST
0405-0284	PR	1		SCREW, 8-18 X 5/8
0405-0474	PR	1		CONICAL WASHER
1149-2109	P	2	E	LOWER HOUSING
1149-2139	C	1	D	PORT COVER
2609-9489	A	1	B	ADHESIVE FOOT
1149-0400	PR	1	B	UL LABEL
1149-0410	PR	1	C	FCC/SERIAL LABEL
1149-9399	PR	1	D	LABEL PLACEMENT DRAWING
1149-0230	A	1	D	INSULATOR, TAPE CONTROL ASSY
0405-0196	PR	1	A	WASHER, FIBRE, FLAT
1149-9269	C	1	C	TRANSFORMER ASSY
1149-2779	C	1	D	TRANSFORMER
1149-2289 *	PR	1	C	FEMALE RECEPTACLE
1149-4489	PR	1	B	TRANSFORMER MOUNTING BRACKET
1149-4839	PR	1	A	RIVET PLATE
0402-0610	PR	1	A	RIVET, SEMI TUBULAR
1149-7809	E	2	D	COMPUTER III ASSY
PL 1149-7809	H	11	A	PARTS LIST,COMPUTER III ASSY
TS 1149-5889	PR	20	A	COMP III ASSY SUBASSY TEST
TS 1149-5679	C	21	A	COMP III ASSY MODULE TEST
TS 1149-5989	Not Rel	19	A	COMP III ASSY SUB ASSY TEST
1149-4589	C	6	D	FABRICATION DRAWING COMP III
1149-9819	A	4(2)	E,RL	SCHEMATIC, COMPUTER III
0099-1360	B	1	B	FERRITE BEAD
1149-7689	PR	1	B	RIBBON CABLE ASSY, POWER, 8 CONDUCTOR
2609-9399	B	1	C	CONNECTOR, 44 PIN EDGE CARD
1149-7699	PR	1	B	RIBBON CABLE ASSY,TAPE, 20 CONDUCTOR
2609-4259	B	1	A	HEAT SINK
1149-7729	PR	1	C	CABLE ASSEMBLY MASTER
1149-2359	C	1	D	CONNECTOR HOUSING
1149-2149	B	1	C	ACCESS PANEL
1149-9369	B	1	C	CONNECTOR ADAPTER ASSY
1149-6369	B	4	C	PRINTED WIRING BOARD, CONNECTOR ADAPTER
1149-7669	PR	1	B	RIBBON CABLE ASSY, TRANSITION, 36 CONDUCTOR
1149-8879	PR	1		BUS BAR, MINI, 2 LAYER
1149-9579	PR	1	B	JUMPER ASSEMBLY
0089-0027 *	PR	1	B	RING TONGUE TERMINAL
0089-0028 *	PR	1	B	POSITIVE LOCK FEMALE RECEPTACLE
0089-0448 *	PR	1	B	WIRE PREPARED, #20AWG, 9 IN
1149-4179	G	1	D	RFI SHIELD, COMPONENT SIDE
1149-4169	E	1	D	RFI SHIELD, CIRCUIT SIDE
1149-4189	C	1	C	RF CLIP

* NORMALLY SUPPLIED AS PART OF NEXT HIGHER ASSEMBLY

<u>DRAWING NUMBER</u>	<u>REV</u>	<u>SHEETS</u>	<u>DWG.SIZE</u>	<u>NOMENCLATURE</u>
1149-9409	E	1	D	TAPE CONTROL ASSEMBLY
PL 1149-9409	E	8	A	PARTS LIST, TAPE CONTROL ASSY
TS 1149-5899	A	5	A	TAPE CONTROL ASSY, SEMI AUTOMATED SUBASSY TEST
TS 1149-5669	C	14	A	TAPE CONTROL ASSY MOD TEST
1149-4409	C	5	D	PRINTED WIRING BOARD, TAPE CONTROL ASSY
1149-9419	C	1	E	SCHEMATIC , TAPE CONTROL ASSY
1149-2039	B	1		KNOB, VOLUME CONTROL
0405-0574	PR	1	A	COMPRESSION RING
1149-7679	PR	1	B	RIBBON CABLE ASSY, POWER, 6 CONDUCTOR
1149-7709	PR	1	B	CABLE ASSY, CONTROL, 9 CONDUCTOR
1149-7599	PR	1	B	CONNECTOR, FEMALE, 9 POSITION
1149-7579	PR	1	A	CONTACT
1149-7719	PR	1	B	CABLE ASSY, CP, 2 CONDUCTOR
1149-7589	PR	1	B	CONNECTOR, FEMALE, 3 POSITION
1149-3239	PR	1	B	BIAS TRANSFORMER
1149-2249	PR	1	C	POTENTIOMETER, VOLUME CONTROL
1149-9219	N	1	D	SWITCHING POWER SUPPLY ASSY
PL 1149-9219	D	8	A	PARTS LIST, SWITCHING PWR SUPPLY
TS 1149-5689	C	10	A	SWX PWR SUPPLY SUBASSY TEST
1149-4219	F	6	D	PCB, SWITCHING POWER SUPPLY
1149-9209	H	1		SCHEMATIC, SWX PWR SUPPLY
1149-9139	A	1	C	BIFILAR WOUND CHOKE
0089-0804	PR	1	B	FUSE CLIP
PL 1149-9998	C	1	A	PKG. PARTS LIST, KEYBOARD COMPONENT
1149-0730	A	1	B	MASTER CARTON
1149-0810	B	1	B	INDIVIDUAL CARTON
1149-0870	PR	1	B	POLY SLEEVE
1149-0920	A	1	A	INSTRUCTION BOOK
1149-2499	PR	2	C	DYNAMIC MICROPHONE
1149-0970	PR	1	A	PACKING SHEET
1149-0860	C	1	C	INSERT (SET OF 2)
1149-0980	A	1	B	KEYBOARD INSERT
1149-9059	E	1	C	CABLE EXTENDER
0001-0820	A	1	A	POLY BAG
0001-6010	A	1	A	POLY BAG
0405-0354	PR	1		SCREW, 8-18 X 1/2
1149-0840	PR	1		INSERT, LEFT
1149-0850	PR	1		INSERT, RIGHT

* NORMALLY SUPPLIED AS PART OF NEXT HIGHER ASSEMBLY

REDUCED COST KEYBOARD

1. Plan
2. Goal
3. Planned Savings
4. Schedule
5. Requirements to meet Goal

REDUCED COST KEYBOARD

Evolution of Present Plan

1. Design Reviews of tape control board & logic board
2. Decision to go to Gate Arrays
3. Investigate Current production yields & problems
 - Master Component compatibility with keyboard
 - Burn in Chamber yields
 - tape deck reliability
4. Prioritizing

TASK		RESPONSIBLE ENGINEER	COST IMPROVEMENT PER UNIT	MATERIAL MAN WEEKS	RATIO COST IMPROV. MAN WEEK	AFFECTS	AFFECTED BY	SCHEDULE:											
								DEC	JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	
A	Logic Board Shields	Al Nash	2.00	5	.4	B													
B	Comp IV & Mega I	Geo Benjamin John Lashman Ward Spantol	21.50	24	.89	A		A	AAFF	FFFF	FFFF	FFFF	FFFF	FFFF					
								AA	AA	FF	FF	FF	FF	FF					
F	Tape Control Card Array	Wilson Quan Joe Dattilio	8.00	16	.5														
G1	Aspec Power Supply	Wilson Quan	16.00	8	2.0														
G2	Current Power Supply Redesign																		
CURRENT PRODUCTION																			
J1	Design Problems	Wilson Quan Fred Klinger John Lashman	2.25	8	.28	J2	J2												
K	Minor Design Changes	John Lashman	.51	3	.17														
N	Master Component Compatibility w/keyboard	Harvey Miller	2.20	1	2.2	J2													
P	Keyboard Subassembly Sourcing	John Lashman	10.00	2	5.0														
TEST ISSUES																			
C	Remove M/C From Burn In	Wilson Quan Bob Balrd	6.32	8	.79														
D	Subassembly Burn In (logic board)	Wilson Quan Gibson Branch	6.98	13	.53	J2													
M	System Test Time Reduction	John Lashman Jim Haupte	3.20	18	.177		J2												
L	Fixture Design For Keyboard Subassembly & Tape Deck	Al Nash	2.00	5	.4														
H	Automated Manufacturing	John Lashman Jim Haupte				J2													
J2	Production Test Issues	Harvey Miller Bob Sternberg Ward Spantol Bob Stello Glenn Branch	5.00																

C = Engineer B = Software Engineer

A = Project Engineer, Manager H = Mechanical Engineer

D = Technician, Model Shop, Artwork Layout F = Outside Service

SCHEDULE:

DEC

JAN

FEB

MAR

APR

MAY

JUN

JUL

AUG

SEP

OCT

REDUCED COST KEYBOARD

GOALS

1. Meet Management objectives to produce 10k to 20k units in June to Dec 82
 - a. No major redesign, subassemblies remain unchanged in function. All redesign activities are independent
 - b. No major housing change and thus no tooling change reqd.
2. Build at lowest practical cost in
 - a. Materials
 - b. Labor

REDUCED COST KEYBOARD

Material Reduction:

1. Quantity buys
2. Logic board size changed
 - a. increase PCBs/Panel from 8 to 12
 - b. reduce parts count
→ improved PCB manufacturability
→ lower cost
3. Use of membrane switch technology for keyboard Subassembly

Logic Board savings goal: \$10 to \$12

LABOR REDUCTION STRATEGY

Design: Reduce pin count wherever possible (eg, 360 to 64)

Subassembly: -Enforce use of Automated incircuit and functional testing

-Pre-burn in subassemblies

Systems -redesign shield on logic board

-reduce systems testing redundancies

-eliminate top housing

RESULTS: =Better yields at Systems Level

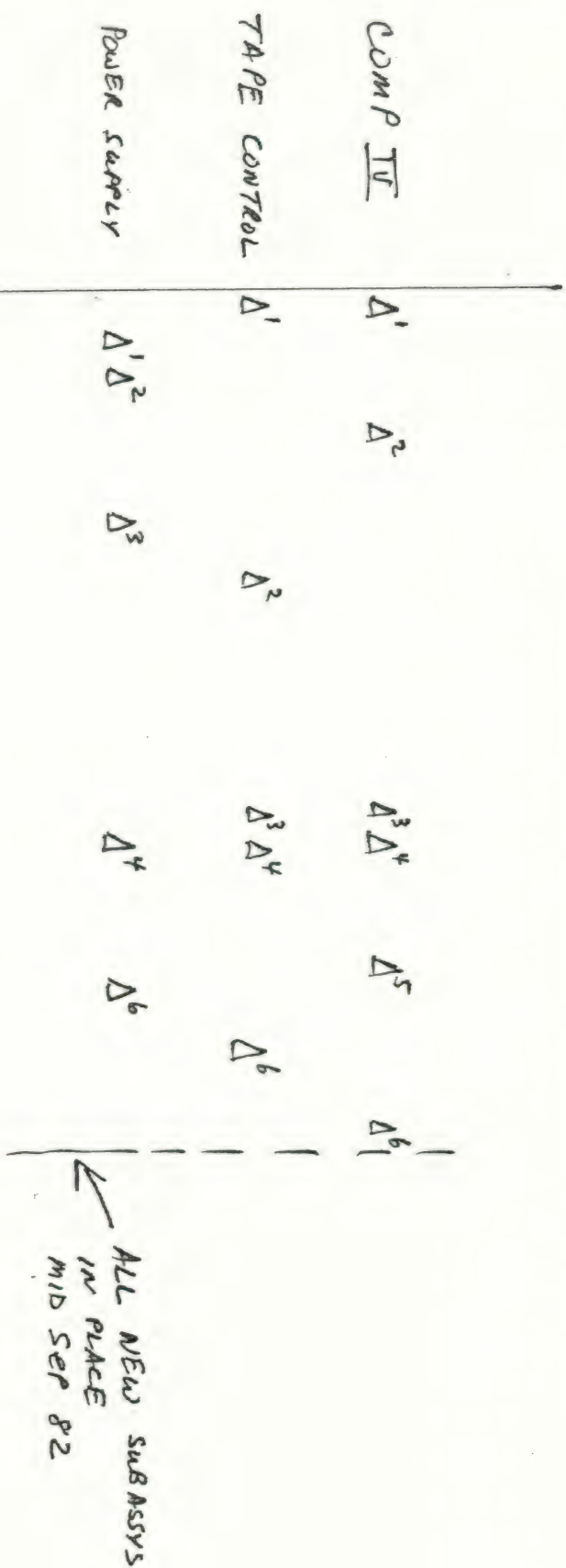
=Less labor required per unit

REDUCED COST KEYBOARD

LABOR: Assembly & Test Time Goals

	<u>Present HPU</u>	<u>Reduced Cost HPU</u>
Logic Board	1.9	1.0
Tape Control	1.3	.7
Power Supply & Transformer	.9	.1
Other subassemblies (preamp/tape deck)	1.7	1.2
Systems Assembly	2.9	1.5
	<hr/>	<hr/>
totals	8.7	4.5

REDUCED COST KEYBOARD SCHEDULE (8 Feb 82)



1. Design Start; specification
2. Place Order, gate array
3. Verify artwork with gate array samples, or verify samples
4. prototype gate array + board, release for production
5. production quantities available..risk samples
6. production quantities

REDUCED COST KEYBOARD

Requirements

1. Resources are not lost to higher priorities
2. Logistics effort receives equal attention as technical effort
3. Determined effort made to insure quality in production process
incoming inspection of components
thorough testing of subassemblies with ATE
4. Follow up & correct deficient processes

Keyboard component address space:

\$0000-\$3FFF Low 8 bits of dual port ram. Used for stack and zpage.

\$4000-\$41FF Internal I/O space

\$4000-\$4007 Read only status bits (read in bit 7)

- \$4000 Data from Cassette
- \$4001 Watermark
- \$4002 End of Tape
- \$4003 Cassette Present
- \$4004 Inter Record Gap
- \$4005 Dropout
- \$4006 Clock Interrupt
- \$4007 Tape Interrupt

\$4020-\$4027 Write only control bits to bit 0 (read will destroy bits)
 \$4040-\$4047 All of these bits are set to zero by system reset.

- \$4020 Enable
- \$4021 Forward
- \$4022 Fast
- \$4023 Record
- \$4024 Mute 1
- \$4025 Mute 2
- \$4026 Mode
- \$4027 Erase
- \$4040 Data to Tape
- \$4041 Tape interrupt enable
- \$4042 External interrupt enable
- \$4043 Blank screen
- \$4044 Keyboard address bit 0
- \$4045 " " 1
- \$4046 " " 2
- \$4047 " " 3

Read Keyboard (read only): The keyboard is read by setting up the address of the desired row in the address bits defined above, and then reading this location will provide the state of the 8 keys in that row. A zero read implies a depressed key.

\$4080 Clear tape interrupt, any access to this location will clear the present tape interrupt

\$40A0 Clear clock interrupt, any access to this location will clear the present clock interrupt

\$40C0-\$40CF CRT controller chip.

- \$40C0 Control register 0, write only, gets \$38
- \$40C1 Control register 1, write only, gets \$23
- \$40C2 Control register 2, write only, gets \$4A, (\$3A)
- \$40C3 Control register 3, write only, gets \$93, (\$97)
- \$40C4 Control register 4, write only, gets \$03
- \$40C5 Control register 5, write only, gets \$3D, (\$7?)
- \$40C6 Last Data register, initially gets \$13, (\$17)

This is the scroll register, and defines the row address of the last line of characters on the screen.

\$40C7 Don't touch!

\$40C8 Cursor column address, read only

\$40C9 Cursor row address, read only

\$40CA Reset the timing chain

RECEIVED
 FEB 28 1980
 C. RUDD

\$40CB
\$40CC
\$40CD
\$40CE
\$40CF

Increment scroll register (last data line)
Write cursor column address, write only
Write cursor row address, write only
Start timing chain
Don't touch

Procedure to start CRT chip is to access the reset location.
Init control registers 0-5 and the scroll register
with the values indicated above (values in () are for 24 data
lines) and then access the start location. Write only
locations will be affected by reads!.

\$40D0
unused chip select

High two bits of dual port ram (bits 0,1 to 6502)

External I/O space

\$B800-\$BFFF

High resolution alpha numeric memory. The memory is mapped
so that address bits 0-5 are column address (0-31) and
bits 6-10 are row address (0-23). If only 20 display lines
are used then clearly rows 20-23 are free for use as
variable ram. Also there are 64 locations which are never
displayed and they also may be used for variable storage.
They are accessed as:

\$BE00-\$BE07
\$BE40-\$BE47
\$BE80-\$BE87
\$BEC0-\$BEC7
\$BF00-\$BF07
\$BF40-\$BF47
\$BF80-\$BF87
\$BFC0-\$BFC7

\$C000-\$DFFF

Program ROM space. Interrupt and reset vectors are at
\$DFFA-\$DFFF

\$E000-\$FFFF

Development and test hardware. This space could also be
used for external software such as BASIC or PASCAL

RECEIVED

FEB 28 1980

C. RUDD

RECEIVED
FEB 28 1980
C. RUDD

	E	D	C	B	A	77	6	5	4	3	2	1	0
		1A DR15	1A DR14	BP1R OUT	BC1 OUT	BC2 OUT	PD7	1REQWA	WC	PD4	PD3	1PATOUT	1BC20
00	0	0	0	0	0	0	0	0	0	0	0	0	1
01	0	0	0	0	1	0	0	0	0	1	0	0	1
02	0	0	0	1	0	0	0	0	0	0	1	0	1
03	0	0	0	1	1	0	0	0	0	1	1	0	1
04	0	0	1	0	0	0	0	0	0	0	0	1	1
05	0	0	1	0	1	0	0	0	0	1	0	1	1
06	0	0	1	1	0	0	0	0	0	0	1	1	1
07	0	0	1	1	1	0	0	0	0	1	1	1	1
10	0	1	0	0	0	0	0	0	0	0	0	0	1
11	0	1	0	0	1	0	0	0	0	1	0	0	1
12	0	1	0	1	0	0	0	0	1	0	1	0	1
13	0	1	0	1	1	0	0	0	1	1	1	0	1
14	0	1	1	0	0	0	0	0	0	0	0	1	1
15	0	1	1	0	1	0	0	0	0	0	0	0	1
16	0	1	1	1	0	0	0	0	0	1	1	0	1
17	0	1	1	1	1	0	0	0	0	1	1	1	1
20	1	0	0	0	0	0	0	0	0	0	0	0	1
21	1	0	0	0	1	0	0	0	0	1	0	0	1
22	1	0	0	1	0	0	0	0	1	0	1	0	0
23	1	0	0	1	1	0	0	0	1	1	1	0	0
24	1	0	1	0	0	0	1	0	0	0	0	1	1
25	1	0	1	0	1	0	0	0	0	0	0	0	1
26	1	0	1	1	0	1	0	0	0	1	1	0	1
27	1	0	1	1	1	0	0	0	0	1	1	1	1
30	1	1	0	0	0	0	0	0	0	0	0	0	1
31	1	1	0	0	1	0	0	0	0	1	0	0	1
32	1	1	0	1	0	0	0	0	1	0	1	0	1
33	1	1	0	1	1	0	0	0	1	1	1	0	1
34	1	1	1	0	0	0	0	0	0	0	0	1	1
35	1	1	1	0	1	0	0	0	0	0	0	0	1
36	1	1	1	1	0	0	0	0	0	1	1	0	1
37	1	1	1	1	1	0	0	0	0	1	1	1	1

Description of the tape format for the Intellivision on-board component

YIELD TAPES FORMAT:

[illegible]

one or more of
hex
binary

NOTIFICATION

A record is defined as an individual followed by data. In order to give the record a chance to lock on to the incoming signal, the first data word is 800 zeros. Their purpose is to ensure that the drive has properly identified the first bit of useful data in the record. There is a pattern which is built into the first criterion for having found a sync pattern. It is to be found in the 800th, 808th, 800th, 800th, or 800th. Thus even if the first five bits of each word are corrected, the drive should still be able to find the sync pattern. The array of 15 bit values added to the record is affected to index into a 1 array of 15 bit values. These 15

The correction scheme is supposed to be able to recover from a loss of any number of bits or words without error. The correction words are not written on the tape as they were written on the tape. The correction words are written on the tape as they were written on the tape. The correction words are written on the tape as they were written on the tape.

A bad 10ms dropout, however, is likely to cause the PLL to lose its data and create a dropout. Even worse, it could cause a sync pattern between each word to be lost. To avoid this, a sync pattern is created by a pattern of bits that can always be uniquely determined, and only a few bits can be lost even by a dropout that covers one of the patterns. Due to this scheme of error recovery, data can only be written on the groups of 32 deletions. Such a group of data gets written on the 32 bits of data, one bit for each word. The bitsync pattern is 5 bits long.

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PRACTICAL CONSIDERATIONS:

When moving in fast forward or in reverse the tape moves at up to 150 inches per second. According to experimental data it takes the drive approximately 500 ms to stop from fast forward to which corresponds to about 1/2 inch of tape. By the time the tape has stopped the drive is already in the initial position at the start of the next scan. The drive will only stop due to a record or a pause in the data. The same holds for a record, so the minimum length of a record is 1/2 inch. The same criterion is met by a record, so the minimum length of a record is 1/2 inch.

LOGICAL TAPE FORMAT:

Because the first foot or so of tape is subject to a great deal of wear, 10 to 20 seconds (above) are left blank at the end of the tape. The definition of a record (above) makes the part of the tape from 10 to 20 seconds of waiting for the data to start. This is avoided by never putting any data in the record. The record is merely a marker. The drive makes it difficult to be sure, after erasing several records, that the tape is positioned before the first record. Every record, the first decade of the number of the record on the tape, and a displacement of the record when reading the record results in an error.

TIMING:

Software:

times; don't necessarily represent physical times
 stop to play: 117ms (hardware about 250ms)
 play to stop: 500ms (hardware about 200ms)

stop to skip forward: 100ms as follows
 skip forward to stop: 400ms

stop to skip forward to stop: 167ms
 skip forward to stop: 133ms (min) in play looking for ing
 skip forward to play: 517ms

stop to skip backward: 100ms
 skip backward to stop: 317ms as follows

stop to skip backward to stop: 83ms
 skip backward to stop: 100ms (min) in play looking for ing
 skip backward to play: 433ms

Approximate hardware times; Time from nominal speed to nominal speed

solenoid delay: 20ms
 stop to play: 250ms
 play to stop: 800ms

stop to fast forward: 500ms
 fast forward to stop: 500ms
 play to fast forward: 400ms
 fast forward to play: 700ms

stop to reverse: 400ms
 reverse to stop: 500ms
 play to reverse: 500ms
 reverse to play: 600ms

fast forward to reverse: 500ms, stopped in 200ms
 reverse to fast forward: 400ms, stopped in 200ms

Description of the tape format for the Intellivision keyboard component

PHYSICAL TAPE FORMAT:

```

<tape> ==> [ <record> ]
<record> ==> "1/3 inch of no data"
<irg> ==> "600 bits of zero"
<phase lock> ==> $0000007E00000000B000000E7
<sync pattern> ==> <sync><bits14><sync><bits13> ... <sync><bits0>
<chunk> ==> %11101
<sync> ==> "bit zero of 32 consecutive correction words"
<bits0> ==>

```

WHERE:

[...] one or more of
\$ hex
% binary

EXPLANATION:

A record is defined as an irg followed by data. In order to give the phase locked loop a chance to lock on to the incoming signal, the first data in a record is 600 zeros. Then, to ensure that the drive has properly identified the first bit of useful data in the record there is a pattern which is very unlikely to occur in any set of random bits, and which can't occur in valid data. The criterion for having found a sync pattern is to have found either \$007E, \$00BD, \$00B, or \$00E7. Thus even given a 10ms (30 bit) dropout in the sync pattern, the drive should still be able to identify it. Each decle of data to be written to the tape is first encoded so that it can be error corrected when read back. The encoding scheme is equivalent to using the decle of data to index into a 1K array of 15 bit values. These 15 bit values are referred to as correction words. Because the correction scheme is supposed to be able to recover from a 10ms dropout anywhere on the tape, correction words are not written on the tape as words since a 10ms dropout would entirely destroy three words of data. Instead 32 words are written on the tape as a group by interleaving the bits, so that the first 32 bits of data would be the high order bits of the first 32 words of data to be written. A 10ms dropout can cause one bit in 30 words to be lost from which the error correction algorithm is able to recover the original data. A bad 10ms dropout however, is likely to cause the PLL to lose or gain a cycle which would cause all the rest of the data on the tape to be misinterpreted. Even were there a sync pattern between each group of 32 words, such a dropout would still cause a sync pattern to be lost. To avoid this problem, each set of 32 bits on the tape is preceded by a pattern of bits the first of which can always be uniquely determined, and only 64 bits can be lost even by a dropout that covers up one of the patterns. Due to this scheme of error recovery, data is only be written on the tape in groups of 32 decles. Such a group of data is referred to as a chunk; one chunk of data gets written on the tape as 55 bits of image data: 15 sets of (bitsync pattern followed by 32 bits of data, one bit from each word in the chunk). The bitsync pattern is 5 bits long.

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PRACTICAL CONSIDERATIONS:

When moving in fast forward or in reverse the tape moves at up to 50ips. According to experimental data it takes the drive appx. 500ms to stop from fast forward directly which corresponds to about 15 inches of tape. By going to fast forward closer to 200ms and the position of the head can be anywhere with respect to the initial position at the start of the procedure. Due to lack of precision in the drive, however, the practical minimum length of an irg is 1 within about 1 or 2 inches, so the practical minimum length of a record is 300 bits. This criterion is met by a record containing 4 chunks.

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LOGICAL TAPE FORMAT:

Because the first foot or so of tape is subject to a great deal of wear, 10 to 20 seconds are left of blank at the beginning of the tape. The definition of a record (above) makes this part of the zeroth record, and an attempt to read this record after rewind would result in 10 to 20 seconds of waiting for the data to start. This is avoided by never putting any data in the zeroth record of tape, but merely using it to skip past to get to the first record of data.

Noise in the drive make it difficult to be sure, after skipping several records, that the tape is positioned before the desired record. Every record, therefore, has a special data chunk referred to as a rib as its first chunk. The first decle of the rib must be the number of the record on the tape, and a disagreement between the record number kept in software and the record number in the rib when reading the record results in an error.

TIMING:

Software times; don't necessarily represent physical times.

stop to play: 117ms (hardware about 250ms)
 play to stop: 500ms (hardware about 80ms)

stop to skip forward: 100ms
 skip forward to stop: 400ms as follows
 167ms in reverse
 100ms in play

skip forward to play: 517ms looking for irg
 133ms (min)

stop to skip backward: 100ms
 skip backward to stop: 317ms as follows
 83ms in fast forward
 100ms in play

skip backward to play: 433ms looking for irg
 133ms (min)

Approximate hardware times; Time from nominal speed to nominal speed.

solenoid delay: 20ms
 stop to play: 250ms
 play to stop: 80ms

stop to fast forward: 500ms
 fast forward to stop: 500ms
 play to fast forward: 400ms
 fast forward to play: 700ms

stop to reverse: 400ms
 reverse to stop: 500ms
 play to reverse: 500ms
 reverse to play: 800ms

fast forward to reverse: 600ms, stopped in 200ms
 reverse to fast forward: 600ms, stopped in 200ms